Appeal Brief Corrected 5/31/00

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of

Applicants	:	Fernando Gonzalez and David Kao
Serial No.	:	09/375,081
Filed	:	August 16, 1999
Title	:	TRANSISTORS HAVING CONTROLLED CONDUCTIVE SPACERS, USES OF SUCH TRANSISTORS AND METHODS OF MAKING SUCH TRANSISTORS
Docket	:	MIO 0007 NA
Examiner	:	G. Munson
Art Unit	:	2811

Assistant Commissioner for Patents
Washington, D.C. 20231

BRIEF ON APPEAL

This is an appeal from the Office Action, mailed March 30, 2000, rejecting claims 15-19 and 23 in the above application. A Notice of Appeal was timely filed on May 4, 2000, with the accompanying fee. Our check in the amount of $300.00 accompanies this Brief in accordance with 37 CFR §1.17(c).

REAL PARTY IN INTEREST

The real party in interest in this application is Micron Technology, Inc. by assignment from the named inventors, and which assignment has been recorded.

RELATED APPEALS AND INTERFERENCES

There are no related cases in which an appeal or interference has been filed.

STATUS OF CLAIMS

Claims 15-19 and 23 are pending in the application.

Claims 15-19 and 23 are rejected.

STATUS OF AMENDMENTS

The application is a continuation of U.S. Patent Application Serial No. 08/987,819, filed December 10, 1997 and issued as a U.S. Patent No. 6,005,273. The application, as filed, included claims 1-32. A preliminary amendment was filed at that time, August 16, 1999 and canceled claims 1-14, 20-22 and 24-32. A supplemental preliminary amendment was filed on November 9, 1999 in which a correction was made to the specification.

SUMMARY OF INVENTION

Referring to figures 1-3 and the specification at page 5, lines 6 et seq, one embodiment of the invention is a multiple gate transistor structure 100. The structure includes a gate structure

104, a secondary oxide layer 116, a spacer 118, a first contact and at least a second contact. The gate structure 104 is formed on a first oxide layer 106 on a semiconductor structure 102 and defines a first gate. The secondary oxide layer 116 is formed over the gate structure. The spacer 118 is formed on at least one side of the gate structure on the secondary oxide layer 116. At least a portion of the spacer 118 is adjacent to the secondary oxide layer 116 being conductive and defining at least a second gate. The first contact 120 is to the gate structure 104. The at least a second contact 122 is to the conductive portion of the spacer.

ISSUES

The following issues define the subject matter of the present appeal:

I. Is the rejection of claims 15, 17, 19 and 23 under 35 U.S.C. § 102 as unpatentable by Rao '139 (U.S. Patent No. 4,213,139) proper?

II. Is the rejection of claims 15-19 and 23 under 35 U.S.C. § 102 as unpatentable by Rao '263 (U.S. Patent No. 4,319,263) proper?

The claims were also rejected under the judicially created doctrine of obviousness-type double patenting. Applicants have filed a terminal disclaimer to overcome that ground of rejection.

GROUPING OF CLAIMS

For the purpose of this appeal claims 15-19 and 23 may be considered in a single group where all of the claims of this group stand or fall together. Claim 15 is exemplary.

ARGUMENT

Applicant's claims 15, 17, 19 and 23 were rejected under 35 U.S.C. § 102 as anticipated by Rao '139 (U.S. Patent No. 4,213,139). Applicant's claims 15-19 and 23 were rejected under 35 U.S.C. § 102 as anticipated by Rao '263 (U.S. Patent No 4,319,263). Rao '263 is a continuation in part of the Rao '139 patent and contains the same disclosure.

The Rao '139 patent discloses a pair of MOS transistors formed as an integrated semiconductor device, sharing a common source/drain region. Each transistor has exactly one gate, and the second gate of the second transistor overlaps the first gate of the first transistor. The Rao '263 patent discloses a plurality of MOS transistors formed as an integrated semiconductor device with adjacent transistors sharing a common source/drain region. Each transistor of the plurality of transistors has exactly one gate. Applicants' invention relates to a multiple gate (i.e. two or more) transistor structure which includes a spacer or gate spacer wherein the spacer takes the form of a second or second and third gates of the transistor.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros. v. Union oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The

identical invention must be shown in as complete detail as is contained in the ... claim." Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

The § 102 rejections above based on Rao '139 and Rao '263 rely on a common rationale in support of rejecting claims 15-19 and 23. This common rationale is that Rao '139 and Rao '263 disclose a multiple gate transistor. However, this rationale is incorrect.

As stated above, claims 15, 17, 19 and 23 were rejected as anticipated by Rao '139. Claim 15 is to a multiple gate transistor and recites "a spacer formed on at least one side of said gate structure ... at least a portion of said spacer adjacent to said secondary oxide layer being conductive and defining at least a second gate." Rao '139 fails to disclose a transistor with at least a second gate. Rao '139 only discloses a pair of transistors wherein each transistor has its own gate. Furthermore, Rao '139 fails to disclose a spacer expressly or inherently. Rao '139 only discloses a second gate of a second transistor overlapping a first gate of a first transistor.

In the Office Action of March 20, 2000, the Examiner argued that Rao '139 disclosed a spacer as the second gate 16 in figures 3 and 5. Applicants respectfully disagree with this statement. As stated above, the second gate 16 of Rao '139 is a gate for a second transistor 11 of Rao '139 and not a gate for the first transistor 10 of Rao '139. Additionally, Rao '139 does not teach a spacer or a conductive spacer as recited in claim 15. Since each and every element of claim 15 is not found, expressly or inherently, in the Rao '139 reference, claim 15 is not anticipated by Rao '139. Applicants respectfully request that this rejection be withdrawn and claim 15 allowed.

Claim 17 is to a two gate transistor structure and recites "a first portion of a spacer formed on a first side of said gate structure on said secondary oxide layer, at least a portion of said first portion of said spacer adjacent to said secondary oxide layer being conductive and defining a second gate." Rao '139 fails to disclose a transistor with two gates. Rao '139 only discloses a pair of transistors wherein each transistor has its own gate. Furthermore, Rao '139 fails to disclose a spacer expressly or inherently. Rao '139 only discloses a second gate of a second transistor overlapping a first gate of a first transistor.

In the Office Action of March 20, 2000, the Examiner argued that Rao '139 disclosed a spacer as the second gate 16 in figures 3 and 5. Applicants respectfully disagree with this statement. As stated above, the second gate 16 of Rao '139 is a gate for a second transistor 11 of Rao '139 and not a gate for the first transistor 10 of Rao '139. Additionally, Rao '139 does not teach a spacer or a conductive spacer as in claim 17. Since each and every element of claim 17 is not found, expressly or inherently, in the Rao '139 reference, claim 17 is not anticipated by Rao '139. Applicants respectfully request that this rejection be withdrawn and claim 17 allowed.

Claim 19 is to an integrated circuit wherein each transistor comprises "a spacer formed on at least one side of said gate structure on said secondary oxide layer, at least a portion of said spacer adjacent to said secondary oxide layer being conductive and defining at least a second gate." Rao '139 fails to disclose a transistor with at least a two gates. Rao '139 only discloses a pair of transistors wherein each transistor has its own gate. Furthermore, Rao '139 fails to disclose a spacer expressly or inherently. Rao '139 only discloses a second gate of a second transistor overlapping a first gate of a first transistor.

In the Office Action of March 20, 2000, the Examiner argued that Rao '139 disclosed a spacer as the second gate 16 in figures 3 and 5. Applicants respectfully disagree with this statement. As stated above, the second gate 16 of Rao '139 is a gate for a second transistor 11 of Rao '139 and not a gate for the first transistor 10 of Rao '139. Additionally, Rao '139 does not teach a spacer or a conductive spacer as in claim 19. Since each and every element of claim 19 is not found, expressly or inherently, in the Rao '139 reference, claim 19 is not anticipated by Rao '139. Applicants respectfully request that this rejection be withdrawn and claim 19 allowed.

Claim 23 is to a transistor structure and includes "a spacer formed on at least one side ... at least a portion of said spacer adjacent to said secondary oxide layer being conductive and defining at least a second gate." Rao '139 fails to disclose a transistor with at least a second gate. Rao '139 only discloses a pair of transistors wherein each transistor has its own gate. Furthermore, Rao '139 fails to disclose a spacer expressly or inherently. Rao '139 only discloses a second gate of a second transistor overlapping a first gate of a first transistor.

In the Office Action of March 20, 2000, the Examiner argued that Rao '139 disclosed a spacer as the second gate 16 in figures 3 and 5. Applicants respectfully disagree with this statement. As stated above, the second gate 16 of Rao '139 is a gate for a second transistor 11 of Rao '139 and not a gate for the first transistor 10 of Rao '139. Additionally, Rao '139 does not teach a spacer or a conductive spacer as in claim 23. Since each and every element of claim 23 is not found, expressly or inherently, in the Rao '139 reference, claim 23 is not anticipated by Rao '139. Applicants respectfully request that this rejection be withdrawn and claim 23 allowed.

Claims 15-19 and 23 were rejected under 35 U.S.C. § 102 as anticipated by Rao '263. Claim 15 is to a multiple gate transistor and recites "a spacer formed on at least one side of said gate structure ... at least a portion of said spacer adjacent to said secondary oxide layer being conductive and defining at least a second gate." Rao 263 fails to disclose a transistor with at least a second gate. Rao '263 only discloses a plurality of transistors where adjacent transistors share a common source/drain region and each transistor has only one gate. Furthermore, Rao '263 fails to disclose a spacer expressly or inherently. Rao '263 only discloses an adjacent gate of an adjacent transistor overlapping a first gate of a first transistor.

In the Office Action of March 20, 2000, the Examiner argued that Rao '263 disclosed a spacer as the second gate 16 and third gate 41 in figures 3, 5 and 7. Applicants respectfully disagree with this statement. As stated above, the second gate 16 of Rao '263 is a gate for a second transistor 11 of Rao '263 and the third gate 41 is a gate for a third transistor 40 and not a gate for the first transistor 10 of Rao '263. Additionally, Rao '263 does not teach a spacer or a conductive spacer as is recited in claim 15. Since each and every element of claim 15 is not found, expressly or inherently, in the Rao '263 reference, claim 15 is not anticipated by Rao '263. Applicants respectfully request that this rejection be withdrawn and claim 15 allowed.

Claim 16 depends from claim 15 and is allowable for the reasons described above. Additionally, claim 16 includes a third gate for the multigate transistor. Rao 236 does not disclose a transistor having three gates. Applicants respectfully request that claim 16 be allowed. Furthermore, claim 16 depends from claim 15 which Applicants have shown to be allowable. Therefore, claim 16 is allowable.

Claim 17 is to a two gate transistor and recites "a first portion of a spacer formed on a first side of said gate structure on said secondary oxide layer, at least a portion of said first portion of said spacer adjacent to said secondary oxide layer being conductive and defining a second gate." Rao '263 fails to disclose a transistor with two gates. Rao '263 only discloses a plurality of transistors where adjacent transistors share a common source/drain region and each transistor has only one gate. Furthermore, Rao '263 fails to disclose a spacer expressly or inherently. Rao '263 only discloses an adjacent gate of an adjacent transistor overlapping a first gate of a first transistor.

In the Office Action of March 20, 2000, the Examiner argued that Rao '263 disclosed a spacer as the second gate 16 and third gate 41 in figures 3, 5 and 7. Applicants respectfully disagree with this argument. As stated above, the second gate 16 of Rao '263 is a gate for a second transistor 11 of Rao '263 and the third gate 41 is a gate for a third transistor 40 and not a gate for the first transistor 10 of Rao '263. Additionally, Rao '263 does not teach a spacer or a conductive spacer as in claim 17. Since each and every element of claim 17 is not found, expressly or inherently, in the Rao '263 reference, claim 17 is not anticipated by Rao '263. Applicants respectfully request that this rejection be withdrawn and claim 17 allowed.

Claim 18 is to a three gate transistor and includes "a first portion of a spacer ... defining a second gate" and "a second portion of said spacer ... defining a third gate." Rao '263 fails to disclose a transistor with three gates. Rao '263 only discloses a plurality of transistors where adjacent transistors share a common source/drain region and each transistor has only one gate.

Furthermore, Rao '263 fails to disclose a spacer expressly or inherently. Rao '263 only discloses an adjacent gate of an adjacent transistor overlapping a first gate of a first transistor.

In the Office Action of March 20, 2000, the Examiner argued that Rao '263 disclosed a spacer as the second gate 16 and third gate 41 in figures 3, 5 and 7. Applicants respectfully disagree with this argument. As stated above, the second gate 16 of Rao '263 is a gate for a second transistor 11 of Rao '263 and the third gate 41 is a gate for a third transistor 40 and not a gate for the first transistor 10 of Rao '263. Additionally, Rao '263 does not teach a spacer or a conductive spacer as in claim 18. Since each and every element of claim 18 is not found, expressly or inherently, in the Rao '263 reference, claim 18 is not anticipated by Rao '263. Applicants respectfully request that this rejection be withdrawn and claim 18 allowed.

Claim 19 is to an integrated circuit wherein each transistor comprises "a spacer formed on at least one side of said gate structure on said secondary oxide layer, at least a portion of said spacer adjacent to said secondary oxide layer being conductive and defining at least a second gate." Rao '263 fails to disclose a transistor with at least two gates. Rao '263 only discloses a plurality of transistors where adjacent transistors share a common source/drain region and each transistor has only one gate. Furthermore, Rao '263 fails to disclose a spacer expressly or inherently. Rao '263 only discloses an adjacent gate of an adjacent transistor overlapping a first gate of a first transistor. In the Office Action of March 20, 2000, the Examiner argued that Rao '263 disclosed a spacer as the second gate 16 and third gate 41 in figures 3, 5 and 7. Applicants respectfully disagree with this argument. As stated above, the second gate 16 of Rao '263 is a gate for a second transistor 11 of Rao '263 and the third gate 41 is a gate for a third transistor 40

and not a gate for the first transistor 10 of Rao '263. Additionally, Rao '263 does not teach a spacer or a conductive spacer as in claim 19. Since each and every element of claim 19 is not found, expressly or inherently, in the Rao '263 reference, claim 19 is not anticipated by Rao '263. Applicants respectfully request that this rejection be withdrawn and claim 19 allowed.

Claim 23 is to a transistor structure and includes "a spacer formed on at least one side ... at least a portion of said spacer adjacent to said secondary oxide layer being conductive and defining at least a second gate." Rao '263 fails to disclose a transistor with at least two gates. Rao '263 only discloses a plurality of transistors where adjacent transistors share a common source/drain region and each transistor has only one gate. Furthermore, Rao '263 fails to disclose a spacer expressly or inherently. Rao '263 only discloses an adjacent gate of an adjacent transistor overlapping a first gate of a first transistor.

In the Office Action of March 20, 2000, the Examiner argued that Rao '263 disclosed a spacer as the second gate 16 and third gate 41 in figures 3, 5 and 7. Applicants respectfully disagree with this argument. As stated above, the second gate 16 of Rao '263 is a gate for a second transistor 11 of Rao '263 and the third gate 41 is a gate for a third transistor 40 and not a gate for the first transistor 10 of Rao '263. Additionally, Rao '263 does not teach a spacer or a conductive spacer as recited in claim 23. Since each and every element of claim 23 is not found, expressly or inherently, in the Rao '263 reference, claim 23 is not anticipated by Rao '263. Applicants respectfully request that this rejection be withdrawn and claim 23 allowed.

Each of the rejected claims recite a spacer which has a specific and known meaning within the art. As stated on page 1, lines 21-22 of the application "spacers formed on the

sidewalls of the gate electrodes of MOS transistors have been utilized in the formation of LDD regions." It is further stated on page 7, lines 19-24 that:

> Where the structure of the transistor 100 is used selectively within an integrated circuit, the remaining devices can be structured as standard LDD transistors using the spacers in a conventional manner. Some or all of the remaining devices can also be conventional transistors without spacers, i.e., not LDD transistors or transistors of the present invention.

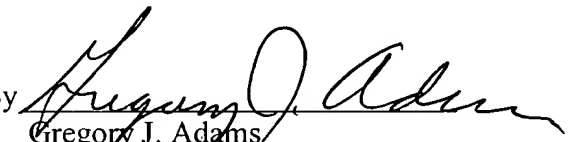
Spacers are semiconductor structures which are typically used in the formation of lightly doped drain transistors. Neither Rao '139 nor Rao '263 include the term "spacer" nor do they teach or suggest a spacer as the term is defined and understood in the art. Rao '139 and '263 only disclose a pair of transistors with overlapping gates. The object of the overlapping gates is to reduce capacitance and provide a small-area series transistor pair. The overlapping gate is not a spacer as is recited in Applicants' claims. Each transistor of Rao '139 or Rao '263 has only one gate whereas for Applicants' invention, each transistor includes a gate and at least one spacer defining at least one additional gate. Claims 15-19 and 23 each recite or depend from a claim which recites a spacer. Since Rao '139 and '263 do not disclose a spacer expressly or inherently, claims 15-19 and 23 are not anticipated by Rao '139 or Rao '263.

Conclusion

For the reasons set forth herein, the Board of Patent Appeals and Interferences is respectfully requested to reverse the decision of the Examiner in rejecting claims 15-19 and 23 of the present application.

Respectfully submitted,

KILLWORTH, GOTTMAN, HAGAN
& SCHAEFF, LLP

By 
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APPENDIX - A
CLAIMS ON APPEAL

15. A multiple gate transistor structure comprising:

a gate structure formed on a first oxide layer on a semiconductor structure and defining a first gate;

a secondary oxide layer formed over said gate structure;

a spacer formed on at least one side of said gate structure on said secondary oxide layer, at least a portion of said spacer adjacent to said secondary oxide layer being conductive and defining at least a second gate;

a first contact to said gate structure; and

at least a second contact to said conductive portion of said spacer.

16. A multiple gate transistor as claimed in claim 15 wherein said spacer is formed on a first side of said gate structure to form a second gate and a second side of said gate structure to form a third gate, said second contact being to said conductive portion of said spacer defining said second gate and said multiple gate transistor further comprising a third contact to said conductive portion of said spacer defining said third gate.

17. A two gate transistor structure comprising:

a gate structure formed on a first oxide layer on a semiconductor structure and defining a first gate;

a secondary oxide layer formed over said gate structure;

a first portion of a spacer formed on a first side of said gate structure on said secondary oxide layer, at least a portion of said first portion of said spacer adjacent to said secondary oxide layer being conductive and defining a second gate;

a first contact to said gate structure; and

a second contact to said conductive portion of said first portion of said spacer.

18. A three gate transistor structure comprising:

a gate structure formed on a first oxide layer on a semiconductor structure and defining a first gate;

a secondary oxide layer formed over said gate structure;

a first portion of a spacer formed on a first side of said gate structure on said secondary oxide layer, at least a portion of said first portion of said spacer adjacent to said secondary oxide layer being conductive and defining a second gate;

a second portion of said spacer formed on a second side of said gate structure on said secondary oxide layer, at least a portion of said second portion of said spacer adjacent to said secondary oxide layer being conductive and defining a third gate;

a first contact to said gate structure;

a second contact to said conductive portion of said first portion of said spacer; and

a third contact to said conductive portion of said second portion of said spacer.

19. An integrated circuit structure comprising:

a first plurality of conventional transistors; and

a second plurality of transistors each comprising:

a gate structure formed on a first oxide layer on a semiconductor structure;

a secondary oxide layer formed on said gate structure;

a spacer formed on at least one side of said gate structure on said secondary oxide layer, at least a portion of said spacer adjacent to said secondary oxide layer being conductive and defining at least a second gate;

a first contact to said gate structure; and

at least a second contact to said conductive portion of said spacer, said first plurality of conventional transistors and said second plurality of transistors being interconnected to form said integrated circuit structure.

23. A transistor structure comprising:

an actual gate and a pseudo gate formed on a first oxide layer on a semiconductor structure, said actual and pseudo gates being separated from one another;

a secondary oxide layer formed over said actual and pseudo gates;

a spacer formed on at least one side of said actual gate and on said pseudo gate on said secondary oxide layer, at least a portion of said spacer adjacent to said secondary oxide layer being conductive and defining at least a second gate;

a first contact to said actual gate; and

a second contact to said conductive portion of said spacer at said pseudo gate.